WHAT IS CLAIMED IS:

1. A semiconductor device that accesses at least one semiconductor storage medium, comprising:

a bus master;

a bus interface that controls access to the at least one semiconductor storage medium based on a request for access to the at least one semiconductor storage medium from the bus master; and

a clock-supply-control circuit that controls the presence of the supply of a clock to the bus master based on access state information that indicates a state of access to the at least one semiconductor storage medium, the clock-supply-control circuit including a circuit that implements at least one of control for stopping the supply of the clock to the bus master if the circuit determines that the bus interface is at a BUSY state, and control for supplying the clock to the bus master if the circuit determines that the bus interface is at a non-BUSY state, based on the access state information.

2. The semiconductor device according to Claim 1, the clock-supply-control circuit implementing a processing to stop the supply of the clock to the bus master after completion of request output from the bus master.

3. A semiconductor circuit that controls a presence of a supply of a clock to a bus master, comprising:

a control-signal generator that generates a clock-supply-control signal for the bus master that instructs the presence of the supply of the clock to the bus master, based on access state information that indicates a state of access to at least one semiconductor storage medium; and

a control circuit that controls the presence of the supply of the clock generated from a clock generator to the bus master, based on the clock-supply-control signal for bus master,

the control-signal generator disabling the clock-supply-control signal for the bus master if access state information indicates that access is in execution; and

the control circuit including a circuit that controls so as to stop the supply of the clock generated from the clock generator to the bus master if the clock-supply-control signal for the bus master is disabled.

4. The semiconductor circuit according to Claim 3, the control-signal generator disabling the clock-supply-control signal for the bus master after the completion of request output from the bus master.

5. Electronic equipment, comprising:

a semiconductor device that includes the semiconductor device according to Claim 1;

a receiving device that receives input information; and

an output device that outputs a result processed by an information-processing device based on the input information.

6. Electronic equipment, comprising:

a semiconductor device that includes the semiconductor device according to Claim 3;

a receiving device that receives input information; and

an output device that outputs a result processed by an information-processing device based on the input information.

7. A method of controlling clock-supply that controls a presence of a supply of a clock to a bus master of a semiconductor device, comprising:

generating a clock-supply-control signal for the bus master that instructs a presence of the supply of the clock to the bus master, based on access state information that indicates a state of access to at least one semiconductor storage medium; and

controlling the presence of the supply of the clock generated from a clock generator to the bus master, based on the clock-supply-control signal for the bus master,

the clock-supply-control signal for the bus master being disabled if access state information indicates that access is in execution; and

control to stop the supply of the clock generated from the clock generator to the bus master being implemented if the clock-supply-control signal for the bus master is disabled.

8. The method of controlling clock-supply according to Claim 6, the clock-supply-control signal for bus master being disabled after a completion of request output from the bus master.